In the Claims

The claims in the listing below will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A method for generating at least one error checking code, comprising:

creating a modified input data word, comprising $(k+m)$ bits, ~~using~~ by combining an input data word, having n-bits, ~~and~~ with at least a previously calculated at least one error checking code, comprising m-bits, where $n \leq k$; and

calculating ~~an intermediate~~ a first m-bit error checking code ~~using~~ from at least a first selected portion of the modified input data word. ~~; and~~

~~generating the at least one error checking code by combining the intermediate m-bit error checking code and a second selected portion of the modified input data word.~~

2. (Original) A method as claimed in claim 1, wherein creating the modified input data word comprises deriving the $(m+n-1)$th to the mth bits of the modified input data word from at least one of the input data word and at least part of the previously calculated at least one error checking code.

3. (Original) A method as claimed in claim 2, wherein creating the modified input data word comprises deriving the $(m+n-1)$th to the mth bits of the modified input data word from at least one of the input data word and the whole of the previously calculated at least one error checking code.

4. (Original) A method as claimed in claim 1, wherein creating the modified input data word comprises deriving the m least or most significant bits of the modified input data word from at least one of m bits, having a predetermined value, and the previously calculated at least one error checking code.

5. (Original) A method as claimed in claim 4, wherein deriving the m least or most significant bits comprises setting at least the n least or most significant bits of the modified data word to the predetermined value.

6. (Original) A method as claimed in claim 5, wherein deriving the m least or most significant bits comprises setting all of the m least or most significant bits of the modified input data word to the predetermined value.

7. (Original) A method as claimed in claim 4, wherein deriving the m least or most significant bits comprises deriving the (m-n) most or least significant bits of the m least or most significant bits of the modified input data word from the previously calculated at least one error checking code.

8. (Currently amended) A method as claimed in claim 1, wherein the first m-bit error checking code is an intermediate m-bit error checking code, and the generating the at least one error checking code comprises performing a finite field arithmetic operation using the intermediate m-bit error checking code and ~~the~~ a second selected portion of the modified input data word to generate the at least one error checking code.

9. (Original) A method as claimed in claim 8, wherein the finite field arithmetic operation comprises at least one of Galois Field (GF) addition or multiplication.

10. (Currently amended) A system for generating at least one error checking code, comprising:

means for creating a modified input data word, comprising (k+m) bits, ~~using~~ by combining an input data word, having n-bits, ~~and~~ with at least a previously calculated at least one error checking code, comprising m-bits, where $n \leq k$; and

means for calculating ~~an intermediate~~ a first m-bit error checking code ~~using~~ from at least a first selected portion of the modified input data word. ~~; and~~

~~means for generating the at least one error checking code by combining the intermediate m-bit error checking code and a second selected portion of the modified input data word~~.

11. (Original) A system as claimed in claim 10, wherein the means for creating the modified input data word comprises means for deriving the (m+n-1)th to the mth bits of the modified input data word from at least one of the input data word and at least part of the previously calculated at least one error checking code.

12. (Original) A system as claimed in claim 11, wherein the means for creating the modified input data word comprises means for deriving the (m+n-1)th to the mth bits of the modified input data word from at least one of the input data word and the whole of the previously calculated at least one error checking code.

13. (Original) A system as claimed in claim 10, wherein the means for creating the modified input data word comprises means for deriving the m least or most significant bits of the modified input data word from at least one of m bits, having a predetermined value, and the previously calculated at least one error checking code.

14. (Original) A system as claimed in claim 13, wherein the means for deriving the m least or most significant bits comprises means for setting at least the n least or most significant bits of the modified data word to the predetermined value.

15. (Original) A system as claimed in claim 14, wherein the means for deriving the m least or most significant bits comprises means for setting all of the m least or most significant bits of the modified input data word to the predetermined value.

16. (Original) A system as claimed in claim 13, wherein the means for deriving the m least or most significant bits comprises means for deriving the (m-n) most or least significant bits of the m least or most significant bits of the modified input data word from the previously calculated at least one error checking code.

17. (Currently amended) A system as claimed in claim 10, wherein the first m-bit error checking code is an intermediate m-bit error checking code, and the means for generating the at least one error checking code comprises means for performing a finite field arithmetic operation using the intermediate m-bit error checking code and ~~the~~ a second selected portion of the modified input data word to generate the at least one error checking code.

18. (Original) A system as claimed in claim 17, wherein the finite field arithmetic operation comprises at least one of Galois Field (GF) addition or multiplication.

19. (Currently amended) A computer program product for generating at least one error checking code, comprising:

a computer readable storage medium having computer readable program code embodied therein, the computer readable program code comprising:

computer readable program code configured to create a modified input data word, comprising (k+m) bits, ~~using~~ by combining an input data word, having n-bits, ~~and~~ with at least a previously calculated at least one error checking code, comprising m-bits, where $n \leq k$; and

computer readable program code configured to calculate ~~an intermediate~~ a first m-bit error checking code ~~using~~ from at least a first selected portion of the modified input data word. ~~; and~~

~~computer readable program code configured to generate the at least one error checking code by combining the intermediate m-bit error checking code and a second selected portion of the modified input data word.~~

20. (Original) A computer program product as claimed in claim 19, wherein the computer readable program code configured to create the modified input data word comprises computer readable program code configured to derive the (m+n-1)th to the mth bits of the modified input data word from at least one of the input data word and at least part of the previously calculated at least one error checking code.

21. (Original) A computer program product as claimed in claim 20, wherein the computer readable program code configured to create the modified input data word comprises computer readable program code configured to derive the (m+n-1)th to the mth bits of the modified input data word from at least one of the input data word and the whole of the previously calculated at least one error checking code.

22. (Original) A computer program product as claimed in claim 19, wherein the

computer readable program code configured to create the modified input data word comprises computer readable program code configured to derive the m least or most significant bits of the modified input data word from at least one of m bits, having a predetermined value, and the previously calculated at least one error checking code.

23. (Original) A computer program product as claimed in claim 22, wherein the computer readable program code configured to derive the m least or most significant bits comprises computer readable program code configured to set at least the n least or most significant bits of the modified data word to the predetermined value.

24. (Original) A computer program product as claimed in claim 23, wherein the computer readable program code configured to derive the m least or most significant bits comprises computer readable program code configured to set all of the m least or most significant bits of the modified input data word to the predetermined value.

25. (Original) A computer program product as claimed in claim 22, wherein the computer readable program code configured to derive the m least or most significant bits comprises computer readable program code configured to derive the (m-n) most or least significant bits of the m least or most significant bits of the modified input data word from the previously calculated at least one error checking code.

26. (Currently amended) A computer program product as claimed in claim 19, wherein the first m-bit error checking code is an intermediate m-bit error checking code, and the computer readable program code configured to generate the at least one error checking code comprises computer readable program code configured to perform a finite field arithmetic operation using the intermediate m-bit error checking code and ~~the~~ a second selected portion of the modified input data word to generate the at least one error checking code.

27. (Original) A computer program product as claimed in claim 26, wherein the finite field arithmetic operation comprises at least one of Galois Field (GF) addition or multiplication.

28. (New) A method as claimed in claim 1, wherein the first m-bit error checking code is an intermediate m-bit error checking code, and the method further comprises generating the at least one error checking code by combining the intermediate m-bit error checking code and a second selected portion of the modified input data word.

29. (New) A method as claimed in claim 1, further comprising calculating the first m-bit error checking code using a parallel CRC module that has one of a k-bit wide data input and a (k+m)-bit wide data input.

30. (New) A method as claimed in claim 1, wherein creating a modified input data word comprises, if n < k, creating the modified input data word such that the (k-n) most significant bits comprise a predetermined value.

31. (New) A method as claimed in claim 1, wherein creating a modified input data word comprises, if n < k, creating the modified input data word such that the (k-n) least significant bits comprise a predetermined value.

32. (New) A method as claimed in claim 1, further comprising creating a first modified input data word, having (k+m) bits, by combining an input data word, having n bits, with an initialization value.

33. (New) A system as claimed in claim 10, wherein the first m-bit error checking code is an intermediate m-bit error checking code, and the system further comprises means for generating the at least one error checking code by combining the intermediate m-bit error checking code and a second selected portion of the modified input data word.

34. (New) A system as claimed in claim 10, further comprising means for calculating the first m-bit error checking code using a parallel CRC module that has one of a k-bit wide data input and a (k+m)-bit wide data input.

35. (New) A system as claimed in claim 10, wherein the means for creating a modified input data word comprises, if n < k, means for creating the modified input data

word such that the (k-n) most significant bits comprise a predetermined value.

36. (New) A system as claimed in claim 10, wherein the means for creating a modified input data word comprises, if n < k, means for creating the modified input data word such that the (k-n) least significant bits comprise a predetermined value.

37. (New) A system as claimed in claim 10, further comprising means for creating a first modified input data word, having (k+m) bits, by combining an input data word, having n bits, with an initialization value.

38. (New) A computer program product as claimed in claim 19, wherein the first m-bit error checking code is an intermediate m-bit error checking code, and the computer program product further comprises computer readable program code configured to generate the at least one error checking code by combining the intermediate m-bit error checking code and a second selected portion of the modified input data word.

39. (New) A computer program product as claimed in claim 19, further comprising computer readable program code configured to calculate the first m-bit error checking code using a parallel CRC module that has one of a k-bit wide data input and a (k+m)-bit wide data input.

40. (New) A computer program product as claimed in claim 19, wherein the computer readable program code configured to create a modified input data word comprises, if n < k, computer readable program code configured to create the modified input data word such that the (k-n) most significant bits comprise a predetermined value.

41. (New) A computer program product as claimed in claim 19, wherein the computer readable program code configured to create a modified input data word comprises, if n < k, computer readable program code configured to create the modified input data word such that the (k-n) least significant bits comprise a predetermined value.

42. (New) A computer program product as claimed in claim 19, further

comprising computer readable program code configured to create a first modified input data word, having (k+m) bits, by combining an input data word, having n bits, with an initialization value.